AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system for maintaining translation consistency in a computer which includes a host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set comprising:

hardware means for providing an indication whether a first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address, the at least one host instruction for execution by the host processor, the hardware means comprising:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the look-aside ~~translation look aside~~ buffer; and

software means for responding to the indication and for assuring that the at least one host instruction will not be utilized once the first memory address has been written, in which the software means removes the at least one host instruction from the second memory address.

2. (Canceled).

3. (Currently Amended) The [[A]] system for maintaining translation consistency as claimed in Claim 1 in which the software means invalidates the at least one host instruction by marking the at least one host instruction at the second memory address.

4-17. (Canceled).

18. (Currently Amended) A memory controller comprising:

an address translation buffer including a plurality of storage locations in which recently accessed virtual addresses are to be recorded and in which physical addresses represented by the virtual addresses are to be recorded, each of the storage locations including means for indicating whether a physical address stores an instruction of a target instruction set which has been translated to an instruction of a host instruction set for execution by a computer system including a host processor, the instruction of a host instruction set for execution by the memory controller; and

means for detecting an indication in a storage location to prevent a write access of the physical address and for indicating a subsequent operation before accessing the physical address, the ~~said~~ means for detecting comprising:

means for generating an exception in response to the detection of the indication; and

means for responding to the exception to indicate the subsequent operation to be taken with respect to the instruction of a host instruction set before accessing the physical address.

19. (Canceled).

20. (Currently Amended) The [[A]] memory controller as claimed in Claim 18 in which the means for indicating comprises a storage position in the storage location.

21. (New) The system for maintaining translation consistency as claimed in Claim 1 wherein the indication comprises a first bit value associated with each of the storage locations in the look-aside buffer.

22. (New) The system for maintaining translation consistency as claimed in Claim 21 wherein a second bit value is also associated with each of the storage locations in the look-aside buffer, the second bit value for indicating a type for a respective physical address, wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address.

23. (New) The system for maintaining translation consistency as claimed in Claim 1 wherein the host processor is a very long instruction word processor and wherein the target instructions comprise x86 instructions.

24. (New) The system for maintaining translation consistency as claimed in Claim 1 further comprising means for detecting the indication to prevent writing the first memory address and for indicating a subsequent operation before accessing the first memory address.

25. (New) The system for maintaining translation consistency as claimed in Claim 24 wherein the means for detecting comprises:

means for generating an exception in response to the detection of the indication; and

means for responding to the exception to indicate the subsequent operation to be taken with respect to the instruction of the host instruction set before accessing the first memory address.

26. (New) The memory controller as claimed in Claim 18 wherein the indication comprises a first bit value.

27. (New) The memory controller as claimed in Claim 26 wherein a second bit value is also associated with the storage location, the second bit value for indicating a type for the physical address, wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address.

28. (New) The memory controller as claimed in Claim 18 wherein the host processor is a very long instruction word processor and wherein the target instruction comprises an x86 instruction.